ABSTRACT

A system and method for accessing a data cache having at least two ways for storing data at the same addresses. A first and second tag memory store first and second sets of tags identifying data stored in each of the ways. A translation device determines from a system address a tag identifying one of the ways. A first comparator compares tags in the address with a tag stored in the first tag memory. A second comparator compares a tag in the address with a tag stored in the second tag memory. A clock signal supplies clock signals to one or both of the ways in response to an access mode signal. The system can be operated so that either both ways of the associative data cache are clocked, in a high speed access mode, or it can apply clock signals to only one of the ways selected by an output from the first and second comparators in a power efficient mode of operation.